

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re patent application of

Kazuki Yokota

Serial No.: Not Yet Assigned

Group Art Unit: Not Yet Assigned

Filing Date: Concurrently Herewith

Examiner: Unknown

For: OVERLAY MARK, METHOD OF MEASURING OVERLAY ACCURACY,
METHOD OF MAKING ALIGNMENT AND SEMICONDUCTOR DEVICE
THEREWITH

Assistant Commissioner of Patents
Washington, D.C. 20231

JC875 U.S. PTO
09/627456
07/27/00
11-2-00

INFORMATION DISCLOSURE STATEMENT

Sir:

Under the provisions of 37 CFR §1.97 through §1.99 and pursuant to applicant's duty of disclosure under 37 CFR §1.56, applicant respectfully brings the following documents listed on the attached form PTO-1449, to the attention of the Examiner in charge of the above-identified application. Copies of the listed documents are provided herewith for the convenience of the Examiner. In compliance with the concise explanation requirement under 37 CFR §1.98(a)(3), the relevance of some of these documents are discussed on pages 2 and 5 of the subject application. Further, English-language Abstracts are attached to the references.

This citation does not constitute an admission that the references are relevant or material to the claims. They are only cited as constituting related art of which the applicant is aware.

It is respectfully requested that the listed references be considered by the Examiner and formally made of record in this application.

Please charge any deficiencies in fees and credit any overpayment of fees to Attorney's Deposit Account No. 50-0481.

Respectfully submitted,

Sean M. McGinn

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Registration No. 34,386

Date:

7/27/00

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